REMARKS

Claims 1-12 and 21-28 were pending in the application. In response to the Office Action mailed October 7, 2002, applicants have canceled claims 1-12 without prejudice or disclaimer, amended claims 21 and 25, and added new claims 29-31. Claims 21-31are now pending for reconsideration.

Claims 1-4, 21-23, and 25-27 are rejected under 35 U.S.C. § 102(e) as being anticipated by Ishinaga (U.S. Patent No. 6,093,940). Claims 5, 7-12, 24, and 28 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishinaga. Applicants respectfully traverse these rejection for the following reasons.

Claims 1-4, 5, and 7-12 are canceled and claim 21 has been amended to obviate this rejection. Claim 25 is maintained as originally presented, although rewritten in independent form.

Claim 21 as amended recites a surface mount light emitting diode package including a plurality of light emitting diode die formed on an integrated circuit substrate. Ishinaga fails to teach or suggest this recited claim feature.

In contrast to the invention as recited in claim 21, Ishinaga teaches only the conventional arrangement, wherein a plurality of separate LED die are utilized in an LED package. Ishinaga discloses that "the two LED elements 2a and 2b are individually fixed" on the substrate (see col. 1, lines 35-37). In fact, Ishinaga teaches away from using a plurality of die from the same substrate. Ishinaga is directed to a two color LED package which uses two different color LED elements (2a is red and 2b is green, see col. 1, lines 65-67). Accordingly, the two die 2a and 2b do not come from the same substrate.

As noted in the specification, there are numerous cost and manufacturing advantages to the device structure recited in claim 21. None of these cost or manufacturing advantages are taught or suggested by Ishinaga.

Because Ishinaga fails to teach or suggest a surface mount light emitting diode package including a plurality of light emitting diode die formed on an integrated circuit substrate, claim 21 and its dependent claims are not anticipated by and are patentable over Ishinaga.

Claim 25 recites a surface mount light emitting diode package including a plurality of LED die which comprise integrally connected adjacent die from a single

wafer. For the reasons given above, the die disclosed in Ishinaga are not integrally connected, are not adjacent, and do not come from a single wafer. Accordingly, the § 102 rejection must be withdrawn. Moreover, as noted in the specification, there are numerous cost and manufacturing advantages to the device structure recited in claim 25. None of these cost or manufacturing advantages are taught or suggested by Ishinaga.

Because Ishinaga fails to teach or suggest a surface mount light emitting diode package including a plurality of LED die which comprise integrally connected adjacent die from a single wafer, claim 25 and its dependent claims are not anticipated by and are patentable over Ishinaga.

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishinaga in view of Yoshida (English abstract of JP Patent No. 05131499). Claim 6 is canceled. Applicants respectfully traverse this rejection as it might be applied to new claims 29-31 for the following reasons.

First, Yoshida fails to make up for the deficiencies of Ishinaga, as described above. Accordingly, claims 29-31 are patentable because their respective independent claims are patentable. Moreover, Yoshida appears to be from a completely non-analagous art of injection molding and is not properly combined with Ishinaga.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. If the rejections are maintained, applicants respectfully request that the Examiner contact the undersigned attorney at the telephone number listed below to arrange a personal interview.

Respectfully submitted,

March 5, 2003
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

-- 21. (Amended) A surface mount light emitting diode package, comprising:

~~a housing~~ an integrated circuit substrate;

a plurality of light emitting diode die ~~supported by~~ formed on the ~~housing~~ integrated circuit substrate; and

a plurality of electrical contacts on the outside of the ~~housing~~ integrated circuit substrate, said contacts adapted for surface mounting to a circuit board and providing electrical signals to said plurality of light emitting diode die.--

-- 25. (Amended) ~~The~~ A surface mount light emitting diode package ~~as recited in claim 21~~, comprising:

a housing;

a plurality of light emitting diode die supported by the housing; and

a plurality of electrical contacts on the outside of the housing, said contacts adapted for surface mounting to a circuit board and providing electrical signals to said plurality of light emitting diode die,

wherein the plurality of die comprise integrally connected adjacent die from a single wafer. --